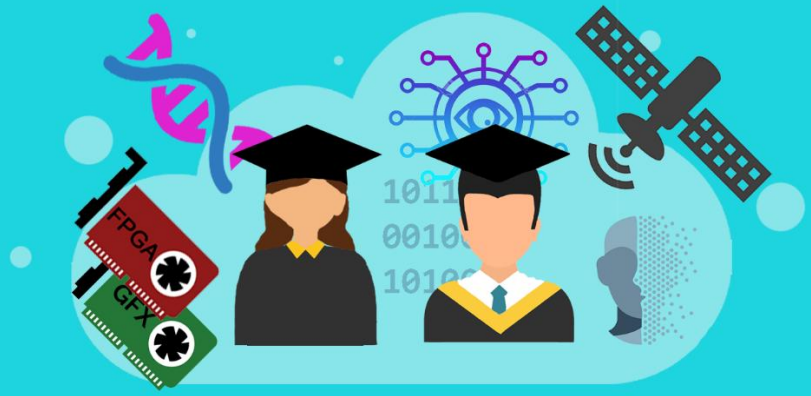




DRAM Modeling for Power, Performance and Area Analysis of Emerging IGZO 2T0C Memories

Conventional DRAM, built from one access transistor and one storage capacitor (1T1C), is approaching its scaling limits. Capacitor and access-transistor leakage, together with growing manufacturing and technology difficulties, make further density gains increasingly hard to achieve [1]. One promising way around these limits is the capacitor-less 2T0C gain cell based on IGZO (indium-gallium-zinc-oxide) transistors. In this cell the storage capacitor is replaced by the parasitic capacitance of the read transistor, while the ultra-low off-current of IGZO gives long retention times (>400 s). IGZO devices can also be fabricated in the back end of line (BEOL), which frees front-end area for the periphery and enables monolithic 3D integration [2]. The 2T0C cell, however, requires more pins and therefore more interconnections than the traditional cell. This thesis will address the system-level impact of these new cell characteristics, by modeling the wiring and the periphery that surround the cell array, since both strongly affect the final power, performance and area (PPA) of the memory.

The main goal of the thesis is to develop a parametric model (C++/Python) that estimates the delay, area and power consumption induced by the interconnects and the periphery of an IGZO 2T0C DRAM, taking layout effects into account and validating the model against circuit simulations with Cadence tools.

Key Aspects:

- **Cell array interconnects:** The new cell array keeps the same topology, but its wiring differs, so the parasitic resistances and capacitances between the nodes of the array must be explored and the macro model fully characterized. Standard schemes for connecting cell subarrays include H-tree configurations, which give symmetrical signals but are slower and more area- and power-hungry, and E-tree configurations, which need less area and delay but can give nodes different timing parameters because of asymmetry.
- **Periphery circuits:** A memory is more than its cell array. The area, speed and power of the periphery, and its connections to the array, must be included. The circuits under investigation are input buffers, write driver circuits, sense amplifiers, equilibration circuits, decoders and pre-decoders, and phase detectors. The diploma thesis focuses on the following areas (but is not limited to):

The diploma thesis focuses on the following areas:

- Modeling and simulating the parasitic RC of the interconnects of the 2T0C cell array, and comparing H-tree and E-tree topologies
- Modeling the delay, area and power of the periphery circuits, including layout effects

- Developing a C++/Python model for the combined wiring and periphery overhead
- Developing automation scripts (Ocean/SKILL) for Cadence simulations and for the interconnection of the different components

RELATED MATERIAL:

[1] "DRAM Scaling Trend and Beyond," TechInsights, <https://www.techinsights.com/blog/dram-scaling-trend-and-beyond>

[2] A. Belmonte, H. Oh, et al., "Capacitor-less, Long-Retention (>400s) DRAM Cell Paving the Way towards Low-Power and High-Density Monolithic 3D DRAM"

[3] A. Belmonte et al., "Tailoring IGZO-TFT Architecture for Capacitorless DRAM, Demonstrating $>10^3$ s Retention, $>10^{11}$ Cycles Endurance and Lg Scalability down to 14 nm," 2021 IEEE International Electron Devices Meeting (IEDM), 2021.

[4] K. Chen et al., "CACTI-3DD: Architecture-level Modeling for 3D Die-stacked DRAM Main Memory," Design, Automation & Test in Europe (DATE), 2012.

[5] B. Keeth, R. J. Baker, B. Johnson and F. Lin, *DRAM Circuit Design: Fundamental and High-Speed Topics*, 2nd ed., Wiley-IEEE Press, 2008

PREREQUISITES:

- VLSI design, Microelectronics
- C++, Python, Bash, Cadence Virtuoso

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