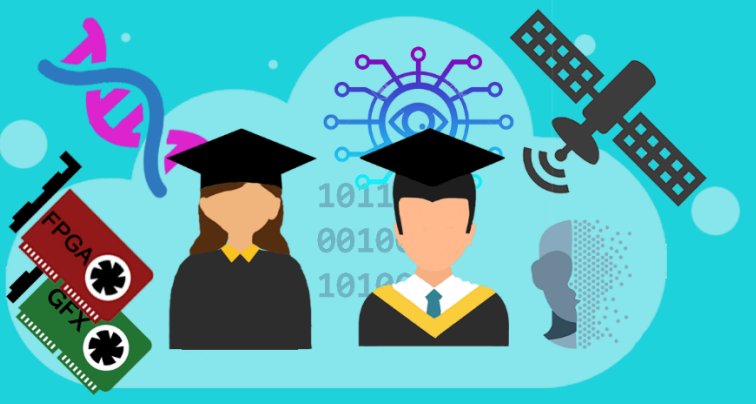
Diploma Thesis

Microproccessors and Digital Systems Laboratory



Multi-Agent AI Systems for Accelerating and Optimizing Integrated Circuit Design

Electronics Design Automation (EDA) tools are the software engines that turn hardware-described designs into manufacturable chips. They contain the full scope of front-end design (specification, RTL capture, simulation, formal verification, synthesis), and back-end physical implementation (floorplanning, placement, routing, timing closure, IR-drop & Electromigration analysis, thermal sign-off) for digital, analog, and mixed-signal systems.

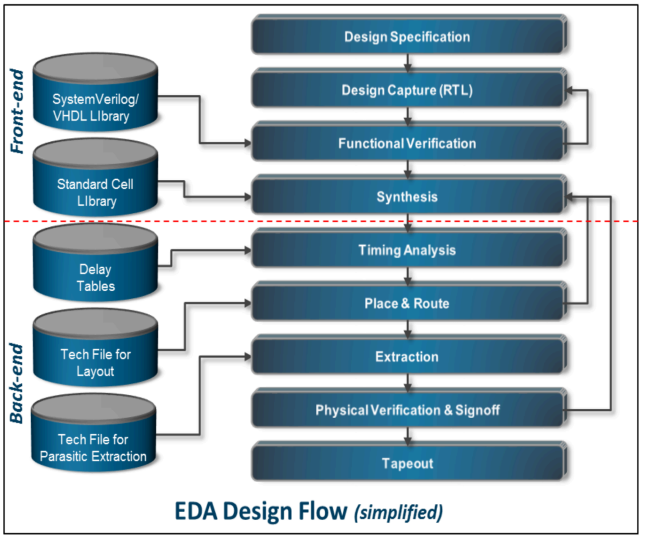


Figure 1: Standard workflow for EDA tools[1]

OpenROAD Framework:

Research interest in **open-source EDA** is rising because it requires no licensing and enables customization for optimizations and PDK support compared to proprietary tools. A key open-source initiative driving innovation in EDA is the OpenROAD project [2]. Its goal is to enable a fully autonomous, open-source RTL-to-GDSII flow, reducing the need for human intervention and drastically cutting design turnaround time. OpenROAD integrates multiple stages of physical design, including floorplanning, placement, clock tree synthesis, routing, and timing analysis. It supports advanced process nodes and provides an accessible platform for research in AI-driven EDA optimization, such as reinforcement learning for placement or generative models for design space exploration

AI Agents in EDA Automation:

The integration of AI agents into EDA workflows can transform how chip design and optimization are approached. These agents leverage machine learning, reinforcement learning, and large-scale data analytics to automate decision-making across multiple design stages. By continuously learning from design feedback (e.g., congestion metrics, timing violations, or power profiles), AI agents can iteratively refine design parameters, improving performance, power efficiency, and area utilization while reducing manual intervention and design turnaround time. Recent research [3], [4] and some commercial efforts [5] focus on using multi-agent systems, where specialized agents cooperate to optimize specific aspects such as placement, routing, or timing closure, ultimately enabling self-optimizing EDA flows that adapt dynamically to design and technology constraints.

The thesis aims to explore how AI agents can coordinate and optimize different stages of the IC design flow. Key optimization steps could potentially include:

- **Design Space Exploration (DSE):** Using AI agents to explore trade-offs between power, performance, and area (PPA) while ensuring design rule compliance.
- **Placement and Routing Optimization:** Reinforcement learning-based agents can predict congestion and timing bottlenecks early, refining placement strategies and routing order for improved timing closure.
- **Synthesis and Floorplanning Feedback:** Agents can integrate feedback from the backend (e.g., PnR congestion or IR-drop data) into front-end synthesis and floorplan decisions to improve design quality iteratively.
- **Collaborative Multi-Agent Optimization:** Multiple agents can specialize in distinct tasks (e.g., placement, routing, and power optimization), sharing insights to accelerate convergence towards optimal design solutions.

RELATED MATERIAL:

[1]https://infohub.delltechnologies.com/nl-nl/l/powerscale-best-practices-for-semiconductor-eda-design-environments/overview-6002/

[2] https://github.com/The-OpenROAD-Project/OpenROAD

[3] AiEDA: Agentic AI Design Framework for Digital ASIC System Design, https://arxiv.org/pdf/2412.09745

[4] ORFS-agent: Tool-Using Agents for Chip Design Optimization, https://arxiv.org/pdf/2506.08332

[5]https://www.prnewswire.com/news-releases/introducing-chipagents-the-worlds-first-ai-agent-for-chip-design-and-verification-302267497.html

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