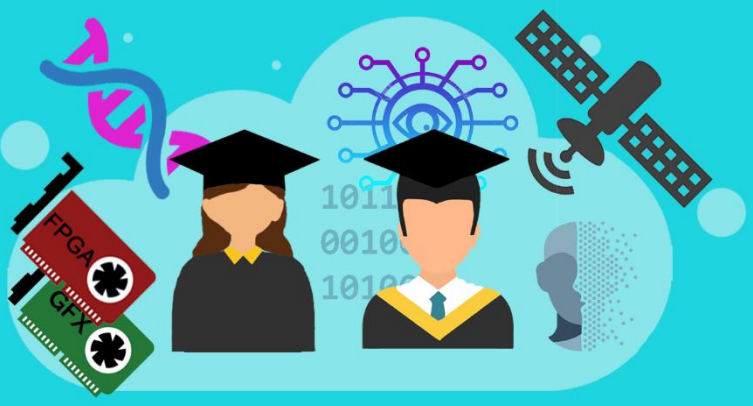
Diploma Thesis

Microproccessors and Digital Systems Laboratory



Development of a Unified UVM–Formal Verification Framework for FPGA and ASIC Design Validation

The focus of this thesis is the integration of Universal Verification Methodology (UVM) and formal verification techniques to create a unified framework for validating complex FPGA and ASIC designs. The goal is to develop a hybrid verification environment that combines the scalability of constrained-random simulation with the exhaustive rigor of property checking, ensuring both functional correctness and corner-case coverage.

This research investigates **methodologies for verification planning, coverage-driven stimulus generation, and assertion-based design validation**, targeting digital subsystems typical of signal processing and embedded computing architectures. The implementation leverages **SystemVerilog UVM for testbench automation** and **formal tools such as SymbiYosys or Siemens Questa PropCheck** for property verification and model checking.

By systematically applying both dynamic and formal techniques, the thesis aims to establish a **complementary verification flow** capable of detecting subtle design inconsistencies early in the development cycle. The resulting methodology will provide a structured approach to **verification reuse, coverage closure, and design reliability**, contributing to more predictable and high-assurance FPGA-based systems suitable for mission-critical and high-performance applications.

PREREQUISITES:

Familiarity with:

- Digital Design and Verification Fundamentals
- Computer Architecture
- Hardware Description Languages (SystemVerilog, Verilog, and/or VHDL)
- Scripting in Python for automation and verification flows
- Version Control Systems (Git)

Desirable:

- Experience with Universal Verification Methodology (UVM)
- Exposure to Formal Verification or Assertion-Based Verification (ABV)
- Use of Simulator Environments (Siemens QuestaSim / ModelSim) Simulator environments (Siemens/Mentor Graphics ModelSim/QuestaSim)
- Knowledge of FPGA Design Flow (e.g., AMD/Xilinx Vivado)
- Understanding of Bus Protocols such as AXI or APB

RELATED MATERIAL:

https://accellera.org/downloads/standards/uvm

https://verificationacademy.com/

https://en.wikipedia.org/wiki/Formal_verification
https://ieeexplore.ieee.org/document/8299595
https://eda.sw.siemens.com/en-US/ic/questa/

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