

Diploma Thesis

Microprocessors and
Digital Systems
Laboratory



Dependability study on RISC-V based GPUs near threshold

The premise of this topic is to utilize the Vortex infrastructure to primarily develop a newly developed Statistical Fault Injection (SFI) model for near-threshold execution and secondarily study circuit dependability by providing an assessment across several axes, from hardware fault injection at different components of the circuit to their final effects in a specific hardware structure. This will lead to a classification of the severity of hardware faults, quantifying the cross-layer vulnerability of the respective hardware structures in fine granularity. Lastly, the criticality of corruptions may also depend on the application at hand, which is also an evaluation axis.

To carry out this cross-layer fault analysis, we employ Vortex as the configurable, full-stack platform for experimentation. Vortex is an open-source, RISC-V based General-Purpose GPU (GPGPU) that supports programming with OpenCL and CUDA. It is designed to facilitate research in GPU architectures by providing a full-stack implementation that includes a minimal instruction set architecture (ISA) extension tailored for GPU operations. Vortex is designed using Verilog and SystemVerilog Hardware Description Languages, making it capable of running on various platforms such as FPGAs and simulators, and is aimed at enabling the execution of OpenCL / CUDA applications in a customizable and scalable environment.

PREREQUISITES:

Familiarity with: Verilog, Python, Bash.

Desirable qualifications: C++, OpenCL.

RELATED MATERIAL:

[AVGI: Microarchitecture-Driven, Fast and Accurate Vulnerability Assessment](#)

[Silent Data Corruptions in Computing: Understand and Quantify](#)

[Veritas – Demystifying Silent Data Corruptions: \$\mu\$ Arch-Level Modeling and Fleet Data of Modern x86 CPUs](#)

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