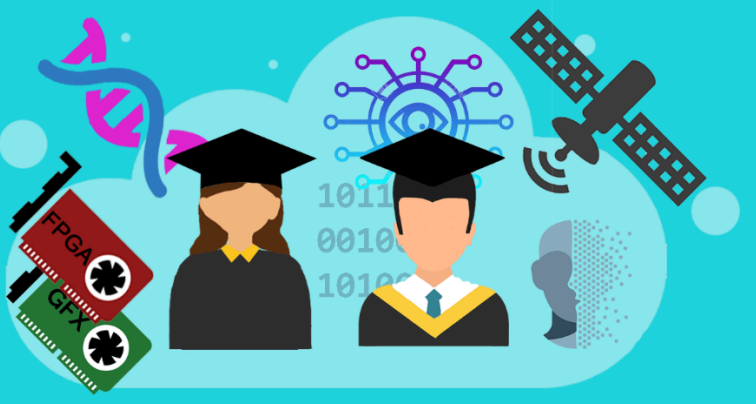
Diploma Thesis

Microproccessors and Digital Systems Laboratory



Heterogeneous RISC-V System on Chip with Hardware Accelerators

Hardware acceleration is one of the most research interesting HW implementations nowadays. The need for performance and energy/area efficiency at the same time led to the implementation of various HW acceleration circuits in different fields of research, with Neural Network accelerators taking the lead. Most of the accelerators implemented have a reusable purpose (a GeMM accelerator can be used by many NN models) but there are also case-specific accelerations as well (in blockchain technologies there are ASIC circuits designed for specific hash functions).

The many different flavors of hardware accelerators (heterogeneity) have a huge need for optimized orchestration. Thus, many groups try to make this happen by utilizing systems where there are host CPUs (mainly RISC-V) that can schedule and control different accelerators. A great example of that is the **SNAX Cluster** implemented by KUL (see more in Related Material).

RISC-V is an open-source instruction set architecture (ISA) based on the RISC principles of simplicity and efficiency. Developed at UC Berkeley, it allows anyone to use and modify it freely, making it popular for applications ranging from embedded systems to high-performance computing.

This thesis aims to develop and evaluate a heterogeneous RISC-V System on Chip (SoC) architecture that integrates multiple hardware accelerators to optimize performance, energy efficiency, and area utilization across a variety of computational tasks. By leveraging the open-source RISC-V (ISA), this research seeks to design a flexible and scalable SoC platform capable of orchestrating diverse accelerators, such as neural networks and cryptographic accelerators, for both reusable and case-specific applications. A key focus of the thesis is the efficient coordination of these accelerators by the RISC-V host CPU to ensure seamless operation, maximizing the potential of hardware acceleration for performance-critical and energy-constrained scenarios. The design and testing of this SoC will provide insights into the orchestration of heterogeneous systems and contribute to advancements in customizable, high-performance computing solutions.

PREREQUISITES:

Familiarity with:

- Computer Architectures
- HDLs (Verilog/VHDL)
- Low-Level Programming (C)

Desirable qualifications:

- Chisel
- Assembly

RELATED MATERIAL:

- https://chipyard.readthedocs.io/en/latest/
- https://www2.eecs.berkeley.edu/Pubs/TechRpts/2016/EECS-2016-17.pdf
- https://boom-core.org/
- https://nvdla.org/
- https://github.com/ucb-bar/gemmini/blob/master/README.md
- https://github.com/KULeuven-MICAS/snax_cluster

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