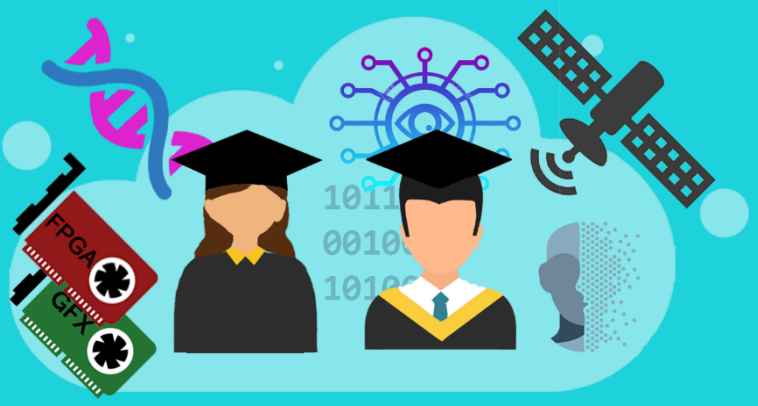
Diploma Thesis

Microproccessors and Digital Systems Laboratory



UVM-Based Verification of a UART IP Core

Hardware Design Verification is a critical process used to ensure that hardware designs function correctly and meet specifications before deployment. The primary goal is to identify and fix design errors early in the development phase, which helps in reducing the cost and time associated with post-deployment fixes.

The principle of hardware verification involves using various techniques and methodologies to thoroughly test and validate hardware designs. Traditional timing simulations, while effective, are often too time-consuming and computationally intensive to rely on solely. Therefore, more advanced verification methodologies are employed to enhance the efficiency and effectiveness of the verification process.

This thesis aims to develop a comprehensive verification environment for a Universal Asynchronous Receiver-Transmitter (UART) IP core using the Universal Verification Methodology (UVM), a standardized framework built on SystemVerilog for verifying integrated circuit designs. The project focuses on building a UVM testbench that thoroughly verifies the UART IP core under various conditions. Key tasks include implementing constrained random stimulus, functional coverage, and assertions to monitor specific behaviors within the design. Additionally, it involves analyzing the performance of the verification environment and documenting the process and results. The ultimate goal is to create an efficient and reliable verification framework that ensures full functional coverage, offering practical insights for industry applications in hardware verification.

PREREQUISITES:

Familiarity with:

- Digital Design
- UART communication protocol
- HDLs (Verilog/VHDL)
- Vivado Toolchain
- Low-Level Programming (C)
- Simulator environments (Mentor Graphics ModelSim/QuestaSim)

Desirable:

- Formal Verification
- SystemVerilog Assertions
- UVM

RELATED MATERIAL:

https://www.chipverify.com/tutorials/systemverilog

https://www.chipverify.com/tutorials/uvm
https://en.wikipedia.org/wiki/Universal_asynchronous_receiver-transmitter
https://repository.rit.edu/theses/9793/

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