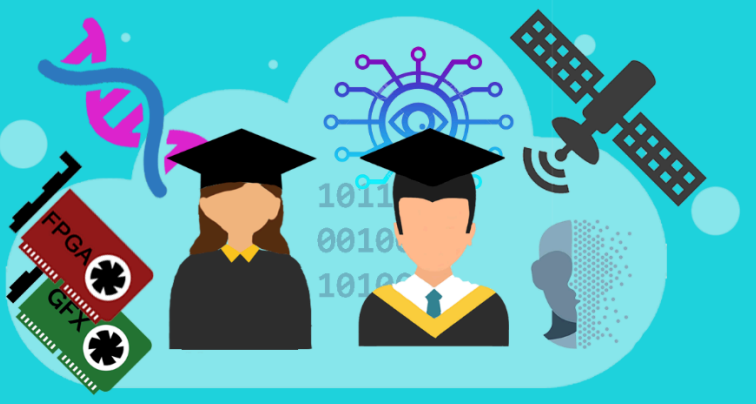
Diploma Thesis

Microproccessors and Digital Systems Laboratory



Impact analysis of micro-architectural changes on power using virtual performance counters

The need for power-efficient circuits nowadays led to the implementation of various power measure features implemented in several microprocessor units. Utilizing those implementations, we can use the measurements in correlation with several events in the circuit to properly model the power, meaning that we can “predict” the power consumption of an architecture based on the events triggered by a certain program. A famous power modeling and dynamic system is the RAPL by Intel (more info in Related Material).

In the lower-power domain, the need for power modeling is a beneficial implementation in order to maintain sustainability when running critical and future-proof applications (Neural Network Models), but we need always to calculate the performance-energy trade-off. The most used CPU architecture for low-power implementations is the RISC-V ISA, which is an open-source instruction set architecture (ISA) based on the RISC principles.

Right now, the RISC-V ISA implements Control and Status Registers (CSRs) to measure certain events in the CPU. Those events can be traced and then correlated with power domain changes or with switching activity among different register paths. This type of measurement though cannot be implemented in a simulated environment, so we need a **proper emulation** of those systems which is usually implemented with FPGAs.

The aim of this thesis is to develop a virtual performance counter system capable of accurately measuring power consumption across different microarchitectural configurations of RISC-V cores, such as variations in branch predictor sizes, load/store queues, and other critical components. By leveraging RISC-V’s Control and Status Registers (CSRs) to track key CPU events, this research seeks to model and predict power consumption in correlation with these architectural parameters. The goal is to create a comprehensive power measurement framework that enables detailed analysis of the performance-energy trade-off in various configurations.

Since such measurements are challenging to replicate in traditional simulation environments, this thesis will also focus on emulating the system using FPGAs to create an accurate testing environment. Ultimately, this work will contribute to optimizing the design of RISC-V cores for energy efficiency and performance balance.

PREREQUISITES:

Familiarity with:

- Computer Architectures
- HDLs (Verilog/VHDL)
- Low-Level Programming (C)
- Kernel Level Development
- Vivado Toolchain

Desirable qualifications:

- Chisel
- Assembly
- I2C Protocol

RELATED MATERIAL:

- https://chipyard.readthedocs.io/en/latest/
- https://www2.eecs.berkeley.edu/Pubs/TechRpts/2016/EECS-2016-17.pdf
- https://boom-core.org/
- https://docs.amd.com/r/en-US/ug480_7Series_XADC/XADC-Overview
- https://docs.amd.com/r/en-US/am006-versal-sysmon/I2C-or-PMBus-Interface
- https://medium.com/@sagarwal3110/measuring-energy-consumption-using-rapl-in-x86-64-cpus-42beb6205f7a

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