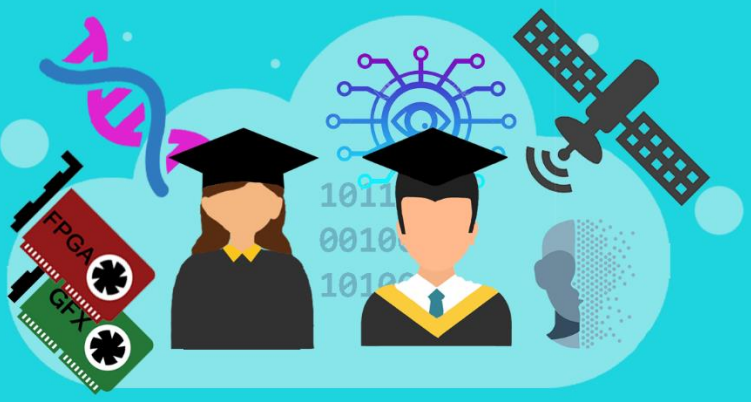
Diploma Thesis

Microproccessors and Digital Systems Laboratory



RISC-V co-processor for AI

Abstract: RISC-V will play a significant role and its base is a compliant core. However it needs high effort to develop and differentiate its feature so that it will become the main selling point. This can be complimented in two ways. Either extending or modifying the instructions of the existing CPU and optimize the AI training model of the target application (i.e motor control). For this concept, a system perspective is an important given that can be applied in automotive domain.
Motivation: The optimization of AI model training by importing additional resources , seems to be receding as a proposed solution which partitions resources (silicon) for motor control + some AI feature. Therefore, the overall aim is to make application performance higher which is sum of all parts i.e. motor control algo + external motor state reading + potential AI model for control or anomaly detection.

Second option is to explore the co-processor route. The stock RISC-V can come from a vendor and differentiating feature could be the co-processor to improve AI + target application performance.

In this thesis the task is to

- Create a performance model for the SoC of scale comparable to our products.
- With functional backend i.e. an ISA to be able to profile workloads to make better co-processor design.
  i. Explore the co-processor route for acceleration of AI workload.
  ii. There is an open HW initiative for defining such interface.
  iii. Evaluate it and try to characterize it.
- Create SoC architecture optimization points by varying options such as
  i. execute from NVM vs SRAM
  ii. performance gain by cache
  iii. dedicated co-processor for removing bottleneck in motor control algorithm.

Rationale for performance model : we will take 3rd party RISC-V so investing time in RTL is not productive, slows simulation and doesn't pay off.
RTL implementation of co-processor still faces the risk to pay for IP developed external to IFX

If you are interested, please email:
NTUA supervisors: Prof. Dimitrios Soudris (dsoudris@microlab.ntua.gr)
Assist. Professor Sotirios Xydis (sxydis@microlab.ntua.gr)
Infineon supervisor: Bhatt Vijay Deep (VijayDeep.Bhatt@Infineon.com)
Department, group and team: Automotive, Smart Power, Product Development