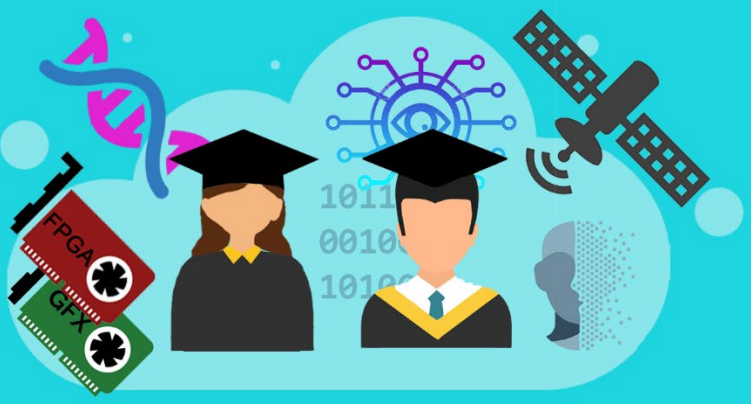
Diploma Thesis

Microproccessors and Digital Systems Laboratory



Replacing Fixed FSMs with Tiny RISC-V Implementations

Abstract The goal is to replace fixed FSMs with tiny, area-efficient RISC-V implementations to achieve flexibility and reusability. This approach eliminates the need to craft a new FSM for each product variant.

Challenges and opportunities While CPUs typically consume more area and power than FSMs, open-source tiny RISC-V implementations have been successfully proven on silicon, achieving areas as small as 0.02-0.06 mm2 at 400 MHz in 65nm tech nodes. By optimizing code implementation, we can reduce memory requirements and make these tiny RISC-V implementations transparent to the product user.

Thesis Objectives

The thesis aims to explore two possible approaches:

- Evaluate Existing Implementations: Use open-source RISC-V implementations to estimate performance and area through synthesis and benchmarking.
- Design a Custom CPU: Design a simple, single- or 2-stage CPU implementing the RV32i base ISA and estimate area through synthesis.

By pursuing either approach, we will gain valuable insights into the most promising tiny cores and determine whether replacing FSMs with tiny RISC-V implementations is a beneficial path to pursue in the future.

If you are interested, please email:
NTUA supervisors
Prof. Dimitrios Soudris (dsoudris@microlab.ntua.gr)
Assist. Professor Sotirios Xydis (sxydis@microlab.ntua.gr)

Infineon supervisor:
Bhatt Vijay Deep (VijayDeep.Bhatt@Infineon.com)
Department, group and team: Automotive, Smart Power, Product Development