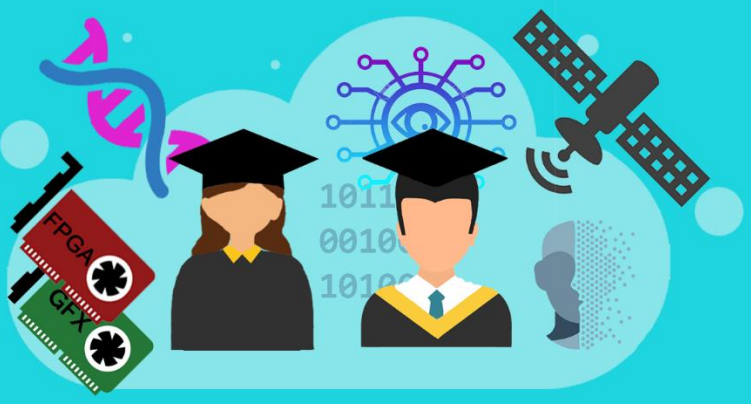
Diploma Thesis

Microproccessors and Digital Systems Laboratory



Transferring knowledge acquired from one FPGA to another

This diploma aims to answer the following question: “Given an application, the applied HLS directives and the corresponding latency and resources for a FPGA, is it possible to estimate the latency and resources for the same directives in another FPGA without performing synthesis?” It is well-known that performing synthesis is a time-consuming process. Over the years, researchers have tried to either minimize the synthesis invocations **[1]** or completely omit them by building model-based approaches **[2]** for the Design Space Exploration (DSE) phase.

In this project, students will transfer knowledge regarding the synthesis points of an application i.e., latency and resources acquired from the MPSoC ZCU104 to other FPGA devices. This will be implemented using a Collaborative Filtering (CF) based model. To build the model Genetic Algorithms (GA) **[3]** will be used to produce synthesis points for different applications on other target devices (e.g., MPSoC ZCU102, Alveo U50). Finally, except from the ML concepts in this project, students will familiarize themselves with Vitis Unified Software Platform **[4]**, the state-of-the-art development tool for accelerating applications using Xilinx FPGAs.

PREREQUISITES:

Strong knowledge of **C/C++**, **Python**, and **Bash Scripting**

Desirable: Familiarity with **High Level Synthesis**, **Machine Learning**, and **Deep Learning**

RELATED MATERIAL:

[1] Xydis, Sotirios, et al. "Compiler-in-the-loop exploration during datapath synthesis for higher quality delay-area trade-offs." ACM Transactions on Design Automation of Electronic Systems (TODAES) 18.1 (2013): 1-35.

[2] Zhong, Guanwen, et al. "Lin-analyzer: A high-level performance analysis tool for FPGA-based accelerators." 2016 53rd ACM/EDAC/IEEE Design Automation Conference (DAC). IEEE, 2016.

[3] https://github.com/aferikoglou/GenHLSOptimizer

[4] https://www.xilinx.com/products/design-tools/vitis/vitis-platform.html

CONTACT INFORMATION:

Aggelos Ferikoglou Ph.D, NTUA (aferikoglou@microlab.ntua.gr)

Dimosthenis Masouros Ph.D, NTUA (dmasouros@microlab.ntua.gr)

Assistant Professor Sotirios Xydis, NTUA (sxydis@microlab.ntua.gr)

Professor Dimitrios Soudris, NTUA (dsoudris@microlab.ntua.gr)