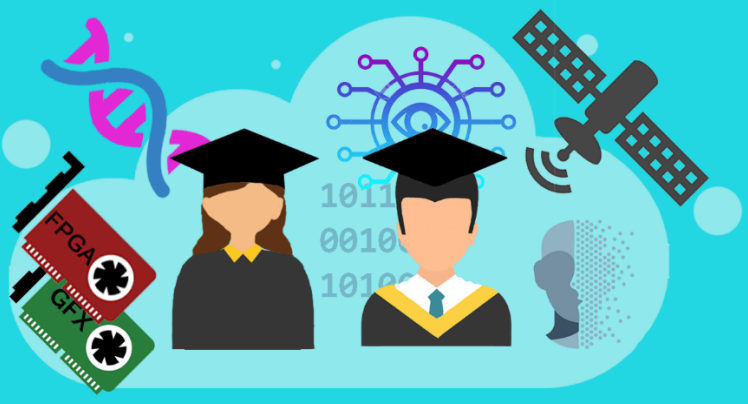
Diploma Thesis

Microproccessors and Digital Systems Laboratory



Lowest-level Software Energy Accounting [HACKERS WANTED]

Last year we issued a call to the arms race for Green Computing. The need for such works has been going up, not down (if you're skeptical about this claim, you can ask someone at least one generation older than you the question "has the weather by any chance *changed* in your lifetime?").

This time around we return with a system-wide vision which we invite you hackers to make a reality: *a self-aware, adaptive, energy-optimal computer.* Imagine a system that knows where energy is spent and why, constantly learning to reconfigure itself (both software- and hardware-wise).

Science fiction? Not quite. Too much for a master's thesis? Of course! But remember: science is incremental. History is written by minimal yet valuable contributions that, by accident or not, are related to each other. This call initiates an effort that will undoubtedly take years to bear, if ever, fruit that is usable for the real world.

We thus propose the following subjects (and kindly ask your input for more):

- **RAPL Reverse Engineering:** students will attempt to produce outputs similar to Intel's RAPL tool [1], using commodity approaches that are already available to the average Linux server. RAPL is, at the time of writing this, the most popular (but proprietary) approach for calculating the energy costs of software at a respectable granularity [2].
- **RAPL Exploitation:** students will generate an open-source framework for the generation of software-energy datasets (preferably on the basic-block level). This should serve as a basis for the exploration of machine learning models that can accurately predict a basic block's energy consumption. Similar work has been done at MIT on the execution time front [3, 4].
- **Energy-measurable RISC-V Softcore:** students will map a Linux-ready RISC-V system on a reconfigurable FPGA, so as to provide the basis for a software interface to the power consumption of several components of interest (CPU, RAM, bus). In contrast to printed systems, FPGAs allow designers to measure power at specific points (power rails). In theory, given the various open-source RISC-V implementations out there, a placement exists that puts said components of interest precisely on these measurable points. Somewhat similar work has been going on at Berkeley [5].

DISCLAIMER:

This is research-level stuff intended for the **seriously passionate**. Once you're in, we will do our best to support and guide you. But the bulk of the work, the debugging sessions and the all-nighters, shall be a burden for your shoulders only. Please understand that you're buying a ticket to Uncertainty Land with this one.

SKILLS YOU WILL NEED:

Demonstrable, ideally through some project of yours, excellent knowledge of Linux and C (for the RAPL-related topics).

For the Softcore, on top of Linux and C, perfect grades on Computer Architecture and VLSI courses, and extreme familiarity with all things FPGA. You need to be comfortable with reading the VHDL/Verilog of a RISC-V implementation, editing it, and loading it on a board.

SKILLS YOU WILL LEARN:

Hopefully the above have got you covered.

RELATED MATERIAL:

[1] H. David, E. Gorbatov, U. R. Hanebutte, R. Khanna and C. Le, "RAPL: Memory power estimation and capping," *2010 ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED)*, 2010, pp. 189-194, doi: 10.1145/1840845.1840883.

[2] Marcus Hähnel, Björn Döbel, Marcus Völp, and Hermann Härtig. 2012. Measuring energy consumption for short code paths using RAPL. *SIGMETRICS Perform. Eval. Rev.* 40, 3 (December 2012), 13–17. DOI:https://doi.org/10.1145/2425248.2425252

[3] Mendis, Charith, et al. "Ithemal: Accurate, portable and fast basic block throughput estimation using deep neural networks." *International Conference on machine learning*. PMLR, 2019.

[4] Chen, Yishen, et al. "BHive: A benchmark suite and measurement framework for validating x86-64 basic block performance models." *2019 IEEE International Symposium on Workload Characterization (IISWC)*. IEEE, 2019.

[5] Keller, Ben, et al. "A RISC-V processor SoC with integrated power management at submicrosecond timescales in 28 nm FD-SOI." *IEEE Journal of Solid-State Circuits* 52.7 (2017): 1863-1875.

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