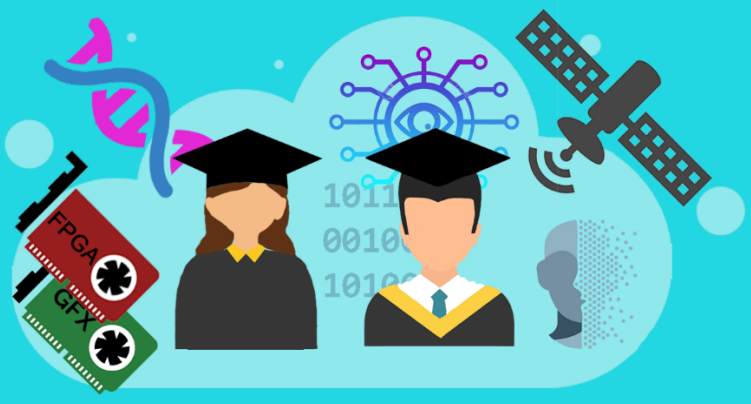
Diploma Thesis

Microproccessors and Digital Systems Laboratory



Novel Out-of-Order GPU Architectures for Deep-Learning Acceleration

GPUs were originally designed for accelerating graphics workloads. Nowadays, due to their massive computing capacity, cost-effectiveness and intuitive programming model, they form the most prevalent platform for accelerating general-purpose workloads. GPUs rely on **massive Thread-Level Parallelism (TLP)** and fast context switching to achieve high resource utilization.

Among the diverse range of general-purpose workloads ported to GPUs, there exists a class of applications or functions (kernels), that fail to support the existing TLP model and suffer from frequent stalling time. These irregular kernels can profit from more **aggressive Instruction-Level Parallelism (ILP)**.

Emerging Out-Of-Order GPU execution schemes exploit ILP, promise improved performance across a wide spectrum of general-purpose and deep-learning applications and pave the way for a complete GPU execution model reshaping.

Accel-Sim and **Multi2Sim** are the cycle-accurate, open-source software packages mostly used and approved by the research community to design and evaluate novel GPU micro-architectural concepts. Our lab is supporting a number of diploma theses that will aim to study, comprehend, improve and extend the boundaries of this fascinating domain of novel GPU architectures.

SKILLS YOU WILL LEARN: The selected candidates will have the chance to (i) familiarize with state-of-art micro-architectural simulators, (ii) dive into the internals of **NVIDIA** and **AMD** GPU architectures and (iii) work on the cutting edge of GPU architecture research.

PREREQUISITES: C/C++, CUDA.

Desirable Qualifications: Python, Bash, familiarity with Linux.

RELATED MATERIAL: 1) Repurposing GPU Microarchitectures with Light-Weight Out-Of-Order Execution 2) Accel-sim, 3) Multi2Sim

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