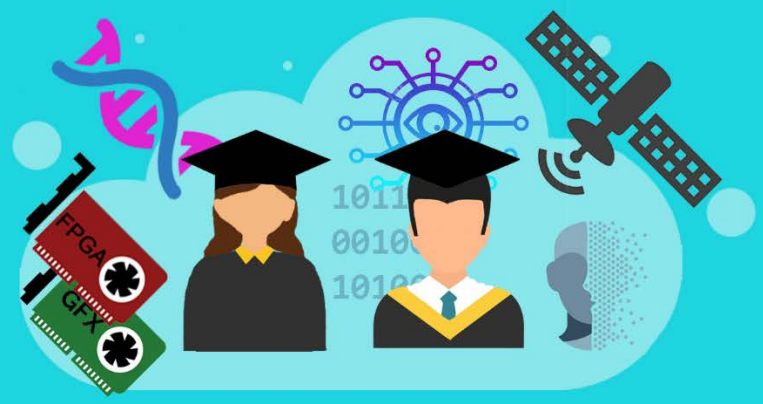
Diploma Thesis

Microproccessors and Digital Systems Laboratory



Porting a framework for Heterogeneous VPUs to RISC-V many-core systems.

The end of Dennard Scaling and miniaturization improvements has led the industry and research to explore new avenues to cope with the increasingly complex new algorithms and applications, like AI. One of the most prominent ways to achieve this is through the introduction of Heterogeneous Computing.

Vision Processing Units or **VPUs** is a new category of specialised and highly heterogeneous many-core processors, both in computational units and in memory, that offer very high performance in a small power envelope. Intel/Movidius Myriad 2 & Myriad X VPUs are some of the best representatives of this category offering 50x increased performance/Watt improvement over traditional CPUs. Leveraging the capabilities of such devices is not an easy task though and requires significant effort from the developer's side as well as in depth knowledge of the underlying hardware.

In an effort to, smoothen the learning curve and increase programmability, microlab is developing a framework named **ParalOS**. The goal of this framework is to achieve the aforementioned features, while also maintaining high performance and allowing low level optimisations.

A new entry to the VPU category is the GreenWaves GAPx series of heterogeneous RISC-V processors featuring the same high level architecture with the Myriad VPUs

The **goal of this diploma thesis** is to port the ParalOS framework a GAP processor, thus creating a common hardware agnostic framework for various VPU architectures.

Keywords

VPU, Heterogeneous Computing, RISC-V, Parallel Programming, Embedded Systems.

Prerequisites

- Good knowledge of C/C++
- Good knowledge of Computer Architecture
- Experience with parallel programming and Operating Systems is a plus.

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