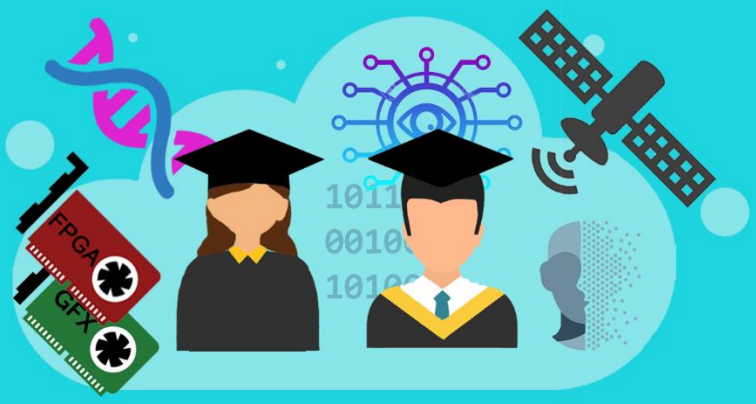
Diploma Thesis

Microproccessors and Digital Systems Laboratory

Academic Year 2019-2020



Implementation of RISC-V Customized Architectures on FPGA Platforms

RISC-V is a novel open-source hardware Instruction Set Architecture (ISA) based on established Reduced Instruction Set Computer (RISC) principles. It was developed at UC Berkeley, aiming to support research in data-parallel architectures. There are many open issues that attract the interest of the research community, e.g., 32/64, Floating-Point, Vector, Atomics, SIMD, etc.

Field Programmable Gate Arrays **(FPGAs)** are semiconductor devices that are based around a matrix of configurable logic blocks, memory and arithmetic resources, all connected via programmable interconnects. FPGAs can be reprogrammed, using the design suite and programming tool provided by FPGA's vendor, to the desired application or functionality requirements after manufacturing.

The **goal of this diploma thesis** is to perform design space exploration and customize the RISC-V version/implementation on FPGA with respect to high-performance applications by exploiting the various parallelization options of this novel architecture.

Useful Links:
https://github.com/riscv/riscv-cores-list
https://en.wikipedia.org/wiki/RISC-V
https://pulp-platform.org/docs/hipeac/pulp_intro_kgf.pdf
https://en.wikipedia.org/wiki/Field-programmable_gate_array

Prerequisites:
basic knowledge of Digital Design, FPGA, VHDL, C

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