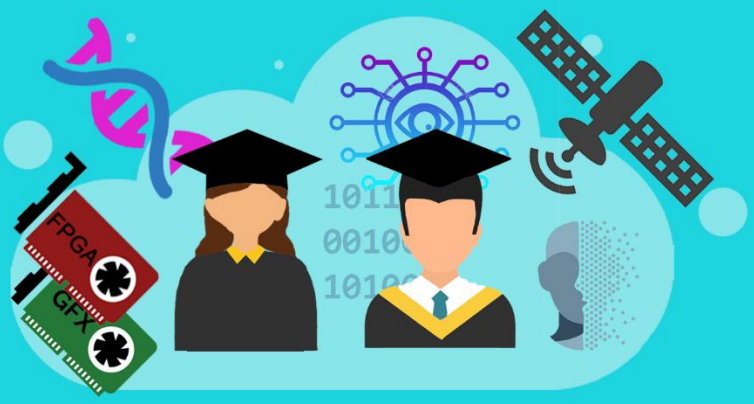
Diploma Thesis

Microproccessors and Digital Systems Laboratory

Academic Year 2019-2020



Customized Redundancy Schemes for Improved Fault-Tolerance of FPGAs in Space Applications

Fault Tolerance is the property of a system to continue operating properly in spite of faults or total failure of some of its components. A fault-tolerant system should be able to handle faults in individual hardware or software components, power failures or other kinds of unexpected disasters, and still meet its specifications. In a broad sense, fault tolerance is associated with reliability, successful and continuous operation and the absence of breakdowns, constraints that must be satisfied in mission-critical systems. Space applications and equipment, which are constantly subject to dangerous environments (e.g., radiation exposure) that may provoke faults on the system, are good examples of this type of system.
The optimal goal of fault tolerance is the development of a reliable system by employing various design approaches and methods, e.g., the traditional triple modular redundancy (TMR) methods consist of triplicating the part of the system to be protected and checking for differences between each output. Moreover, the development of a fault-tolerant system involves tasks, such as the **Fault Injection**, i.e., the insertion of user-defined faults for testing purposes, or **Error Detection and Correction**.

Field Programmable Gate Arrays **(FPGAs)** are semiconductor devices that are based around a matrix of configurable logic blocks, memory and arithmetic resources, all connected via programmable interconnects. FPGAs can be reprogrammed, using the design suite and programming tool provided by FPGA's vendor, to the desired application or functionality requirements after manufacturing.

The **goal of this diploma thesis** is to explore novel redundancy schemes and develop frameworks/methodologies to customize any given FPGA implementation with respect to power/throughput/resource minimization.

Useful Links:
https://pld.ttu.ee/IAF0530/draft.pdf
https://en.wikipedia.org/wiki/Fault-tolerant_computer_system
https://en.wikipedia.org/wiki/Fault_injection
https://en.wikipedia.org/wiki/Error_detection_and_correction
https://en.wikipedia.org/wiki/Field-programmable_gate_array

Prerequisites:
basic knowledge of Digital Design, FPGA, VHDL, C

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