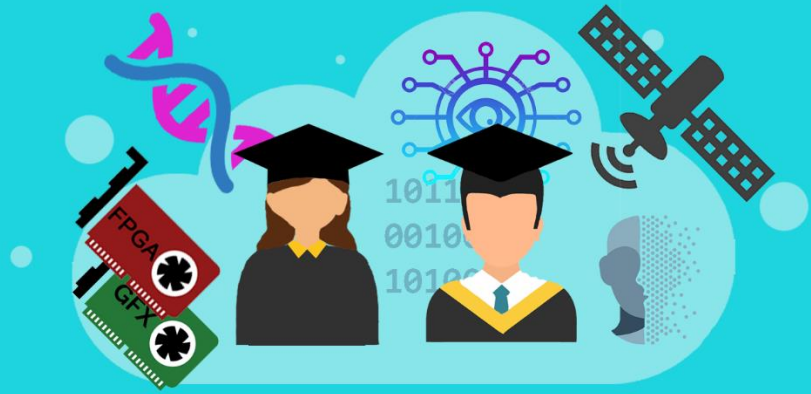


Diploma Thesis

Microprocessors and
Digital Systems
Laboratory



Constrained design of heterogeneous many-core systems

The current trend in modern computing systems is to integrate hardware accelerators for optimizing specific applications related mostly on machine learning and artificial intelligence. Even though, the accelerators can offer us tremendous speed-up in specific use cases, they are not flexible and they cannot be utilized in all situations. For example, an accelerator cannot be shared at the same time by multiple applications. These constraints require the development of a methodology that generates architectures with integrated accelerators under specific constraints.

The goal of this thesis is to develop practical methods for automatic generation of customized heterogeneous architectures. Given (i) a library of accelerators (ii) a set of representative applications with extracted power and performance profiles; (iii) The total area capacity of the chip A_{total} ; and (iv) Power constraints of the chip, develop a systematic methodology that (i) finds the number and types of accelerators cores per cluster; and (ii) develop run-time resource management techniques.

PREREQUISITES:

Good knowledge of C/C++, computer architectures

READING MATERIAL:

1. Co-designing accelerators and SoC interfaces using gem5-Aladdin
2. LASER: A hardware/software approach to accelerate complicated loops on CGRAs

CONTACT INFORMATION:

Prof. Iraklis Anagnostopoulos: (iraklis.anagno@siu.edu)

Prof. Dimitrios Soudris: (dsoudris@microlab.ntua.gr)