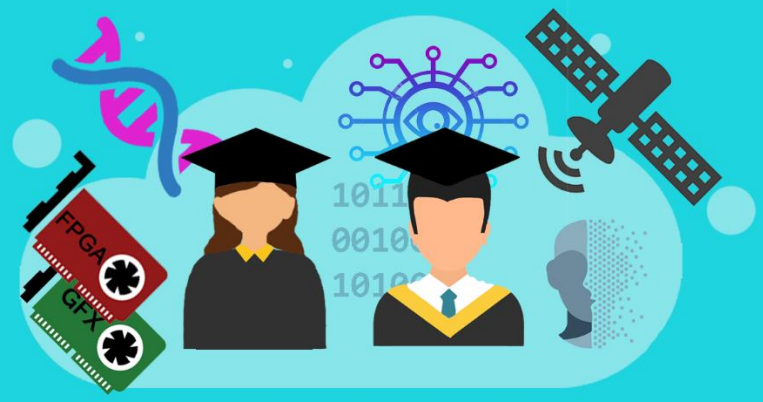
Diploma Thesis

Microproccessors and Digital Systems Laboratory



Constrained design of clustered asymmetric many-core systems

Platform heterogeneity prevails as a solution to the power/performance problem imposed by parallel applications and technology scaling. Even though heterogeneity can be applied in multiple forms, such as functional heterogeneity by employing coprocessors, specialized accelerators, reconfigurable fabrics etc., the performance and power limitations are driving the emergence of micro-architectural heterogeneity in terms of asymmetric cores, also known as iso-ISA cores. In these systems, processing elements have the same Instruction Set Architecture (ISA) but differ in terms of performance and power properties, thus allowing the same executable to run on different cores to reduce power. An extension of this architecture is clustered asymmetric multicore systems, where cores of the same type are clustered together sharing a last level cache, memory controller, voltage-frequency levels etc. but different clusters can have different characteristics (e.g. size of cache, types of cores).

The goal of this thesis is to develop practical methods for automatic generation of customized architectures. Given (i) *a library of asymmetric cores with different performance and power properties*; (ii) *a set of representative applications with extracted power and performance profiles*; (iii) *The total area capacity of the chip* A_{total}; and (iv) *Power constraints of the chip, develop a systematic methodology that* (i) finds the number and types of cores per cluster; and (ii) customizes the inter-cluster architecture (e.g. LLC size, number of memory controllers) such that: (1) Application contention is minimized; (2) The applications' performance requirements are met; (3) The total area of all the selected cores is less than Atotal; and (4) The generated configuration meets the power constraints imposed by the selected technology

Reading material

1. Hades: Architectural synthesis for heterogeneous dark silicon chip multi-processors

2. A design space exploration methodology supporting run-time resource management for multi-processor Systems-on-chip

Requirements

Good knowledge of C/C++, computer architecture.

Tools: Sniper many core simulator, Hotsniper

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